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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,499	01/22/2002	Jin-Yuan Lee	JCLA8534	7456
27765	7590	03/01/2006	EXAMINER	
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			THAI, LUAN C	
			ART UNIT	PAPER NUMBER
			2891	

DATE MAILED: 03/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,499	LEE ET AL.	
	Examiner	Art Unit	
	Luan Thai	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 2/8/06.
- 2a) ☒ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 281-286 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 281-286 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office action is responsive to the RCE filed 2/08/06.

Claims 281-286 are pending in this application.

Claims 1-280 have been cancelled.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 281 is rejected under 35 U.S.C. 102(b) as being anticipated by Sakurai (6,078,104 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding 281, Sakurai (see specifically figures 1-3, Col. 3, line 27 to Col. 7, line 25) disclose a method for fabricating an electronic component comprising: joining a die (1) and a substrate (5), wherein the die (1) has a top surface at a horizontal level; and after the joining the die and the substrate, depositing a bump (6/66) over the horizontal level (Col. 6, lines 39+), wherein the bump (6/66) comprises gold (Col. 6, lines 35+).

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3. Claim 282 is rejected under 35 U.S.C. 102(b) as being anticipated by Wojnarowski et al. (5,576,517).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding 282, Wojnarowski et al. (see specifically figure 2) disclose a method for fabricating an electronic component comprising: depositing an insulating layer (20) over a die (14), wherein the insulating layer (20) comprises a porous structure (Col. 5, lines 10+).

4. Claim 283 is rejected under 35 U.S.C. 102(b) as being anticipated by Kunimatsu et al. (5,767,564).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 283, Kunimatsu et al. (see specifically figure 1) disclose a method for fabricating an electronic component, comprising: joining a die (2) and a substrate (1), wherein the die (2) has a top surface at a horizontal level, and after joining the die (2) and the substrate (1), depositing a passive device (e.g., capacitor 3) over the horizontal level (Col. 3, lines 34+).

5. Claim 284 is rejected under 35 U.S.C. 102(e) as being anticipated by Yoshimura et al. (6,690,845).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 284, Yoshimura et al. (see specifically figure 176) disclose a method for fabricating an electronic component, comprising: providing a die (904) having a top surface at a

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horizontal level; and depositing a waveguide (1005) over the horizontal level (Col. 65, lines 51+).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 285 is rejected under 35 U.S.C. 103(a) as being unpatentable over Felton et al. (6,759,273).

Regarding claim 285, Felton et al. disclose (see specifically figures 1-8) a method for fabricating an electronic component comprising: providing a wafer (1) having a top surface at a horizontal level; depositing micro electronic mechanical sensors (MEMS) (5) over the horizontal level (Col. 9, lines 22+), and dicing the wafer to produce a plurality of MEMS dies (17), each of which has a micro electronic mechanical sensor depositing on the die (Col. 9, lines 56+). Thus, Felton et al. teach depositing micro electronic mechanical sensors on a wafer, instead of on a die (a piece being cut from a wafer) as applicant claimed, and then dicing the wafer to produce a plurality of MEMS dies.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made modify the method of Felton et al. by dicing the wafer into plurality of dies and forming the MEMS individually, instead of forming in mass produce, since

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the process of making individual MEMS is simpler and within the ordinary designing ability expected of a person skilled in the art.

8. Claim 286 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger (5,111,278 of record) in view of Fasano et al. (6,139,666) .

Regarding claim 286, Eichelberger discloses (see specifically figure 17) a method for fabricating an electronic component comprising: depositing an insulating layer (208) over a circuitry element (e.g., chip 204 or wiring 201), planarizing the insulating layer (208) by lapping (Col. 24, lines 1-11), and depositing a metal layer (209) over the insulating layer (Col. 23+). Eichelberger teaches lapping the insulating layer (208), instead of grinding the insulating layer, as applicant claimed.

Fasano et al. teach both lapping and grinding processes are commonly used in the art for planarizing a surface (Col. 2, lines 58+ and lines 50+). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply grinding process (instead of lapping) to planarize the insulating layer in Eichelberger structure since the examiner takes Office Notice of the equivalence of grinding method and lapping method for their use in planarizing a surface in the art (as disclosed by Fasano et al.) and the selection of any of these known equivalents to planarize a surface would be within the level of ordinary skill in the art.

9. The following reference(s) is/are cited as of interest to this application:

U.S. Pat. No. 6,486,535 of record (Col. 5, lines 26+) is cited for showing that the passive devices may include capacitors, resistors, inductors arranged as filters to suppress power source noises and attain speed-up of the operation of the chip.

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U.S. Pat. No. 6,614,110 of record (Col. 4, lines 10+) is cited for showing that a MCM (multi-chip module) is common to comprise integrated circuit chips, passive devices, and a MEMS.

U.S. Pat. No. 6,205,032 of record (Col. 4, lines 32+) is cited for showing that waveguides can be considered as passive devices.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:30 AM - 5:00 PM, Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Luan Thai

Primary Examiner

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February 23, 2006